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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,302	07/02/2003	Kang Yong Kim	501313.01	4303

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EXAMINER

NGUYEN, MINH T

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/613,302

Applicant(s)

KIM ET AL.

Examiner

Minh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-60 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/10/03</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses words which can be implied, i.e., "Embodiments of the present invention", "is provided". Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claims 1, 10, 18, 27, 45 and 57 are objected to because of the following informalities:

In claim 1, lines 11-12, "the coarse delay circuit" should be changed to -- the reference coarse delay component --, see line 5.

In claim 10, line 14, "the adjustable delay circuit" should be changed to -- the adjustable delay stage -- for consistent, see line 2.

In claim 18, lines 18-19, "the coarse delay circuit" should be changed to -- the reference coarse delay component --.

In claims 27 and 45, same problems exist as discussed in claim 18.

In claim 45, line 3, --by-- should be inserted after “input clock signal”.

In claim 57, line 3, , --by-- should be inserted after “input clock signal”.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 13, 21, 30 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 4, the recitation “a signal stabilization circuit coupled to the feedback circuit” is misdescriptive because the recited “signal stabilization circuit” is inside the feedback circuit. The terms “stabilized compensation signal” and “control signal” appear the same signal. Clarification is requested.

As per claims 13, 21, 30 and 39, the same problem exists to each of these claims as noted in claim 4.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims discussed below are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,327,318, issued to Bhullar et al.

As per claim 1, Bhullar discloses a compensation circuit (Fig. 5) for an adjustable delay circuit having fine and coarse delay circuits (this is merely the intended use of the compensation circuit, however, it can be seen in Fig. 3, elements 13 and 15), comprising:

a reference delay circuit (29, 39A and 39B) receiving an input clock signal (DIV_CLK) and outputting a reference delayed clock signal (REF_CLK), having a reference fine delay component (39A and 39B) and a reference coarse delay component (29), the time delay of the coarse delay component greater than the time delay of the fine delay component (as the names suggested) and having an expected relationship with respect to the time delay of the fine delay component (these delays are fixed);

an adjustable fine delay circuit (31A and 31B, controllable by the decoder 37) having a control terminal (for receiving the signals from the decoder 37), receiving the input clock signal (DIV_CLK) at an input and outputting a variable delayed clock signal (the signal from 31B to

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the phase detector 33), having a time delay adjusted according to the control signal provided by the detector (37);

a phase detector (37) having a first input coupled to the output of the coarse delay circuit and a second input coupled to the output of the adjustable fine delay circuit (as shown) to compare the phase relationship of the reference delayed clock signal and the variable delayed clock signal (this is the function of a phase detector), the phase detector generating an output signal (UP and DN); and

a feedback circuit (35 and 37) coupled to the phase detector (33) to generate a compensation signal (the control signal) indicative of the variance from the expected relationship between the time delay of the coarse and fine delay components, the feedback circuit further providing the compensation signal to the adjustable fine delay circuit as the control signal.

As per claim 2, the recited shift register reads on the binary counter (35), column 5, lines 62-66, note that a binary counter is a form of a shift register.

As per claim 4, insofar as understood, the recited signal stabilization circuit reads on the decoder (37), and the compensation signal, the stabilized compensation signal and the control signal are the signal used to adjust the adjustable fine delay circuit (31A and 31B).

As per claim 7, see column 4, lines 26-29, i.e., “inverters” (plural, more than one) and “in series”.

As per claim 9, the coarse delay component (CDE, 29) and the fine delay component (FDE3, 39A) are connected as recited.

As per claim 10, this claim is rejected for the same reasons noted in claim 1. The recited adjustable delay stage, first and second reference delay stages, latch circuit are the adjustable fine

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delay circuit, reference fine and coarse delay components and phase detector of claim 1, respectively.

As per claims 11, 13 and 17, these claims are rejected for the same reasons noted in claims 2, 4 and 9, respectively.

As per claim 18, this claim is rejected for the same reasons noted in claim 1, and further, Fig. 3 shows the DLL recited in the preamble, the recited variable delay line reads on the delay elements 13 and 15, the recited delay controller reads on the decoders 9 and 11.

As per claims 19, 21, 24 and 26, these claims are rejected for the same reasons noted in claims 2, 4, 7 and 9, respectively.

As per claim 27, this claim is rejected for the same reasons noted in claim 18, and further, the limitations recited on the first nine lines of the claim are met since these are standard elements in a memory device, see column 1, last paragraph of the Bhullar reference.

As per claims 28, 30, 33 and 35, these claims are rejected for the same reasons noted in claims 2, 4, 7 and 9, respectively.

As per claim 36, this claim is rejected for the same reasons noted in claim 27, and further, the limitations recited on the first four lines of the claim are met since these are standard elements in a computer system.

As per claims 37, 39, 42 and 44, these claims are rejected for the same reasons noted in claims 2, 4, 7 and 9, respectively.

As per claims 45-60, these claims are merely a method to operate the compensation circuit having the structure recited in claim 1, since Bhullar teaches the circuit, the method is inherently disclosed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims discussed below are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,327,318, issued to Bhullar et al.

As per claim 3, Bhullar explicitly discloses the shift register (35) is a six-bit shift register (column 5, lines 63-66) in a preferred embodiment but he does not explicitly disclose the shift register is a three-bit shift register as called for in the claim.

The examiner takes Official Notice the fact that the more number of bits, the finer control of the delay. It also notorious well-known that the more number of bits used, the more expensive the overall circuit becomes because more registers are needed. Also, producing several versions of a product, high end and low end, is a common practice in the industry.

It would have been obvious to one skilled in the art at the time of the invention was made to reduce the number of bits in the Bhullar compensation circuit from six bits to three bits to reduce the cost of the overall circuit so that the circuit can be used in a low end product.

As per claim 6, Bhullar discloses the phase detector (33) but he does not disclose the detail implementation of the detector which comprises a SR latch and a buffer as called for in the claim.

The examiner takes Official Notice the fact that such a structure of a phase detector is old and well-known in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to implementing the Bhullar phase detector using a latch and a buffer. Because the structure is well-known and popular used in the industry, one can avoid the time necessary to design a phase detector.

As per claim 8, Bhullar discloses the structure of the reference delay circuit which comprises a coarse delay connected to a fine delay whereas the claim calls for a fine delay connected to a coarse delay.

However, it has been ruled by the court, it is not inventive to rearrange the parts in a circuit when general condition is met.

It would have been obvious to one skilled in the art at the time of the invention was made to switch the location of the reference fine and coarse delays in the Bhullar circuit, the motivation would be to reduce the interference problem if during the assembly process, the artisan determines that such an arrangement reduces the EMI problem.

As per claims 12 and 15-16, these claims are rejected for the same reasons and motivation noted in claims 3, 6 and 8, respectively.

As per claims 20, 23 and 25, these claims are rejected for the same reasons and motivation noted in claims 3, 6 and 8, respectively.

As per claims 29, 32 and 34, these claims are rejected for the same reasons and motivation noted in claims 3, 6 and 8, respectively.

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As per claims 38, 41 and 43, these claims are rejected for the same reasons and motivation noted in claims 3, 6 and 8, respectively.

Allowable Subject Matter

6. Claims 5, 14, 22, 31 and 40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

These claims are allowable because the prior art of record fails to disclose or suggest the inclusion of a flip-flop, a NOR gate and an inverter in at least one stabilization stage as recited in each of these claims.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to be 'Minh Nguyen', followed by the date '4/9/02' written in a similar cursive style.

Minh Nguyen
Primary Examiner
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